WHAT IS CLAIMED IS:

1. A test circuit for a microcontroller unit, comprising:

a first pin receiving a first signal;

a second pin receiving a second signal; and

a test signal generating circuit that generates a test signal in response to a logical combination of the first signal and the second signal.

2. The circuit of claim 1, wherein the test signal generating circuit comprises:

a logic circuit that logically processes the first signal and the second signal;

a counter that is enabled and disabled based on an output signal from the logic circuit, wherein the test mode counter uses the second signal as a counting signal when enabled; and

a decoder that outputs the test signal when a count value from the counter reaches a prescribed count value.

3. The circuit of claim 2, wherein the test mode counter is disabled and reset when the output signal from the logic circuit is a low level.

4. The circuit of claim 3, wherein the logic circuit is an OR-gate, and wherein the first and second signals are a clock signal, and a reset signal, respectively.

5. The circuit of claim 1, further comprising:

a test mode related circuit operated by the first signal and the second signal; and

an internal circuit that enters a test mode in accordance with the test signal from the test signal generating circuit.

6. The circuit of claim 5, wherein the internal circuit operates in a second mode when the count value reaches a second prescribed count value.

7. The circuit of claim 1, wherein the first signal is a high level in the test mode.

8. A microcontroller unit having a test mode setup circuit, the test mode setup circuit comprising:

a clock pin that receives a clock signal;

a reset pin that receives a reset signal;

a test mode counter that is set and reset based on the clock signal and the reset signal, wherein the set test mode counter counts the reset signal; and

a decoder that receives a count value from the test mode counter and activates a test mode flag when the count value reaches a prescribed value.

9. The microcontroller unit of claim 8, further comprising a test mode related circuit operated by the clock signal and the reset signal that outputs a test signal based on the test mode flag.

10. The microcontroller unit of claim 9, further comprising an internal circuit that enters a test mode in accordance with the test signal.

11. The microcontroller unit of claim 8, wherein the clock signal is a high level in the test mode.

12. The microcontroller of claim 8, further comprising:

a clock pin receiving a clock signal;

a reset pin receiving a reset signal; and

an OR gate ORing the clock signal and the reset signal.

15. The microcontroller unit of claim 10, further comprising a logic gate that logically combines the clock signal and the reset signal.

16. The microcontroller unit of claim 15, wherein the test mode counter is reset when an output value from the logic-gate is a low level, and wherein the logic-gate is an OR gate.

17. A test mode setup circuit for a microcontroller unit, comprising:

a clock pin that receives a clock signal;

a reset pin that receives a reset signal;

a test signal generator that counts the reset signal in accordance with a logical combination of the clock signal and the reset signal to generate a test signal, wherein the test signal generator comprises,

a logic gate that logically processes the clock signal and the reset signal,

a test mode counter that is set and reset in accordance with an output signal from the logic gate to count the reset signal and output a count signal, and



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a decoder that outputs a test signal when the count signal from the test mode counter is a prescribed value; and

a test mode related circuit operated by the clock signal and the reset signal that enters an internal circuit into a test mode in accordance with the test signal from the test signal generator.

18. The circuit of claim 17, wherein the clock signal is a high level in the test mode, wherein the logic-gate is an OR-gate, and wherein the test mode counter is reset when an output value from the OR-gate is a low level.

19. The circuit of claim 17, wherein the test mode related circuit enters the internal circuit into a second mode when the count signal reaches a second prescribed value.